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CATV MAX3509 +68dBmV Cable Telephony Upstream Solution

This application note presents design modifications to increase the output signal from the MAX3509 cable upstream amplifier, making it support circuit switched cable telephony systems. The amplifier has sufficient gain to produce 66dBmV. Details are given to address output return loss, thermal reliability and harmonic distortion.

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Applications Technical Support

Introduction

Circuit switched cable telephony applications require a large upstream signal to overcome coupler loss (Figure 1). The MAX3509 can drive high output power while maintaining low harmonic distortion and compliance to data over cable service interface specification (DOCSIS). Figure 4 shows modifications to the MAX3509 EV Kit to achieve high power.

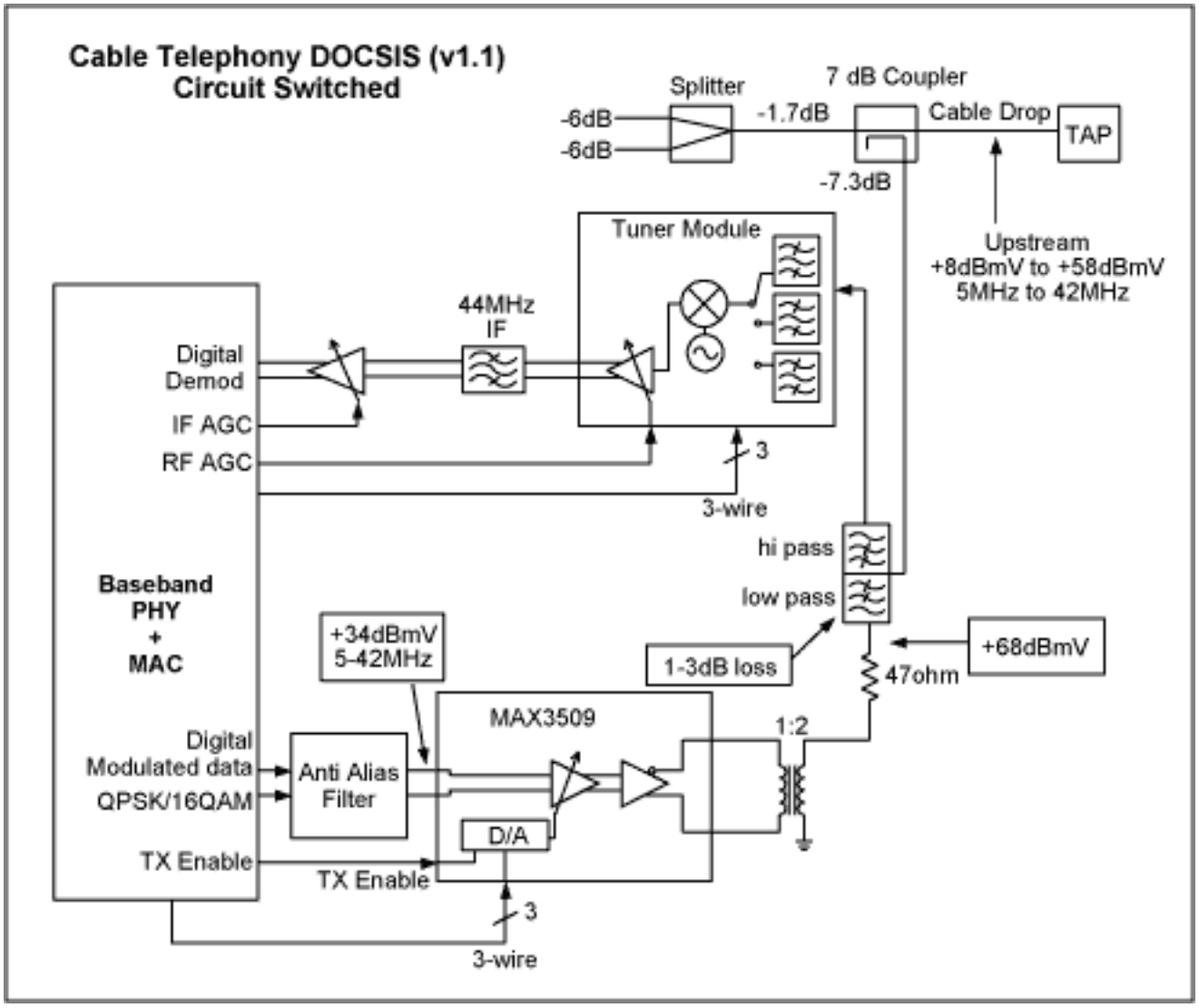

Figure 1. Cable telephony block diagram

The MAX3509 Overview

The MAX3509 is a programmable power amplifier for use in CATV upstream applications. It features variable gain controlled by a 3-wire digital serial bus. Gain control is available in 1dB steps. The device operates over a 5MHz to 65MHz frequency range. The MAX3509 offers a transmit-disable mode, which places the device in a high-isolation state for use between bursts in TDMA systems. In this mode, all analog functions are shut down, minimizing output noise and power consumption. When entering and leaving transmit-disable mode, transients are kept to 25mV nominal at full gain. In addition, supply current is reduced to 7.8mA.

The power amplifier has two current-feedback amplifiers in an instrumentation amplifier configuration. This architecture provides superior even-order distortion performance but requires an external transformer to convert to a single-ended output. In transmit-disable mode, bias to the power amplifier is reduced to a minimal level, which provides high input to output isolation and low output noise.

The MAX3509 has sufficient gain to produce an output level of 66dBmV (1:1 transformer) when driven with a 34dBmV input signal. Rated performance is achieved with this input level. When a lower input level is present, the maximum output level will be reduced proportionally and output linearity will improve. If an input level greater than 34dBmV is used, distortion performance degrades.

Output Return Loss

DOCSIS requires a 6dB return loss on the upstream path from 5MHz to 42MHz. When used with a coupler this is easily met. The return loss is already 14dB for a 7dB coupler (Figure1) no matter what the output impedance of the upstream amplifier is.

The MAX3509 has a 1.2Ω output impedance in transmit mode and 170Ω in transmit disable mode. This output impedance is transformed by a 1:4 impedance ratio (N = 1:2 voltage) by the MAX3509 output transformer (in this case, a Toko 458PT-1087). The equivalent source impedance of the MAX3509 and output transformer can be calculated by observing Figure 4. In transmit mode the 1.2Ω output impedance is transformed to 4.8Ω in series with a 47Ω resistor or 51.8Ω. In transmit disable mode the 170Ω output impedance is transformed to 680Ω in series with a 47Ω resistor or 727Ω.

Safe Operating Area

A current feedback amplifier will drive as much current as it takes to maintain output voltage. This has the benefit of achieving low distortion into a dynamic load. However, a low impedance load will draw more current from the amplifier. Therefore, one must be aware of power consumption and power dissipation. The duplex filters first element is typically a shunt capacitor that will reduce output load impedance and increase current draw. The lowest impedance the upstream amplifier will drive will most likely be at the duplex filter band edge of 42MHz.

Continuous power dissipation for the MAX3509 is 2200mW at +70° C and de-rated by 27mW/° C above 70° C. This is based on JEDEC equivalent PCB. The maximum I_{CC} that can be drawn with a JESD51-7 equivalent PCB at 85° C and V_{CC}=9V would be (2200 - (85 - 70) 27)/9 = 199mA.

Depending on board layout and output loading it is possible to safely increase the maximum current draw (Icc) by using a heat sink. The MAX3509 maximum junction temperature limitation is +150° C and θjc = 2.43° C/W.

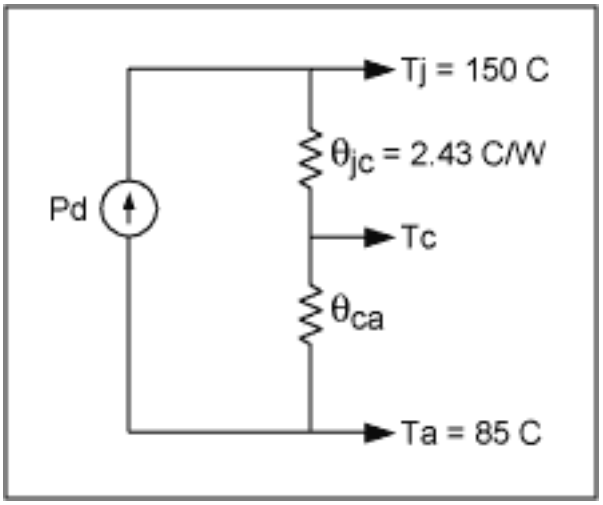

Figure 2 Power dissipation

For example, if it was found that the MAX3509 drew 230mA at 42MHz, 70dBmV output and an ambient temperature of 85° C, one could calculate the heat sink requirements as follows:

Determine Pd = V_{CC} ▪ I_{CC} = 9V ▪ 230mA = 2070mW. Calculate θjc + θca = (Tj - Ta)/Pd = (150 - 85)/2.070 = 31.4C/W. Subtract θjc to get θca = 28.97C/W. θca is the thermal dissipation of the heat sink. The heat sink is most commonly designed with the surrounding metal chassis. 95% of the heat flow is through the exposed paddle on the bottom of the MAX3509. A thermal plane directly under the exposed paddle running to a heat sink will be the most effective dissipater of heat. Additionally via's from the thermal plane to the ground plane can help increase heat dissipation by increasing surface area of the thermal plane. A temperature measurement at the case (Tc) can confirm proper heat sink design. One would measure the temperature as close to the exposed paddle as possible to determine case temperature. Note, the top of the MAX3509 has very little thermal conductivity. Placing a heat sink on top of the part would not be effective.

There are three basic ways to reduce power dissipation of the MAX3509.

1. Operate at a lower output power.
2. Operate into larger output impedance.
3. Operate at a lower V_{CC}.

This design has utilized all three. First, it is operating at a reduced output power of +67dBmV (See Figure 6). Secondly, a series 47Ω output resistor has been added to increase the output impedance. Thirdly, data has been taken at 8.3V (a diode drop below 9V) to observe a 100mW power savings without much effect on harmonics (See Figure 10,11).

To operate without compromise in performance heat sinking is the best option.

System Design

The end goal is to be compliant with DOCSIS. One of the major stumbling blocks is the spurious emission requirement. Figure 3 shows the DOCSIS integrated spurious emissions limit. The tough operating condition to overcome is the full power (+58dBmV) spurious emission limit for the frequency bands of 54MHz to 60MHz and 60MHZ to 88MHz. Figure 3 shows that 93dBc and 98dBc of suppression is needed respectively! Since the in-band spurious emission limit (5 to 42MHz) is -47dBc it will be quite common to have -50dBc harmonics from the amplifier both in band and out of band. The duplex filter is then used to attenuate the out of band harmonics. In order to design the duplex filter one needs 2nd and 3rd harmonic distortion data of the upstream amplifier (MAX3509) plus the system specification (DOCSIS see Figure 3) to determine the design goal attenuation of the duplex filter.

For a differential bipolar product, such as the MAX3509, third harmonic distortion tends to be the limiting factor verses the second harmonic distortion. The two critical points for third harmonic distortion are fo = 18MHz (54MHz 3rd) and fo = 20MHz (60MHz 3rd). Figure 6 shows third harmonic distortion for 22MHz, which is close enough to 18MHz, and 20MHz for all practical purposes.

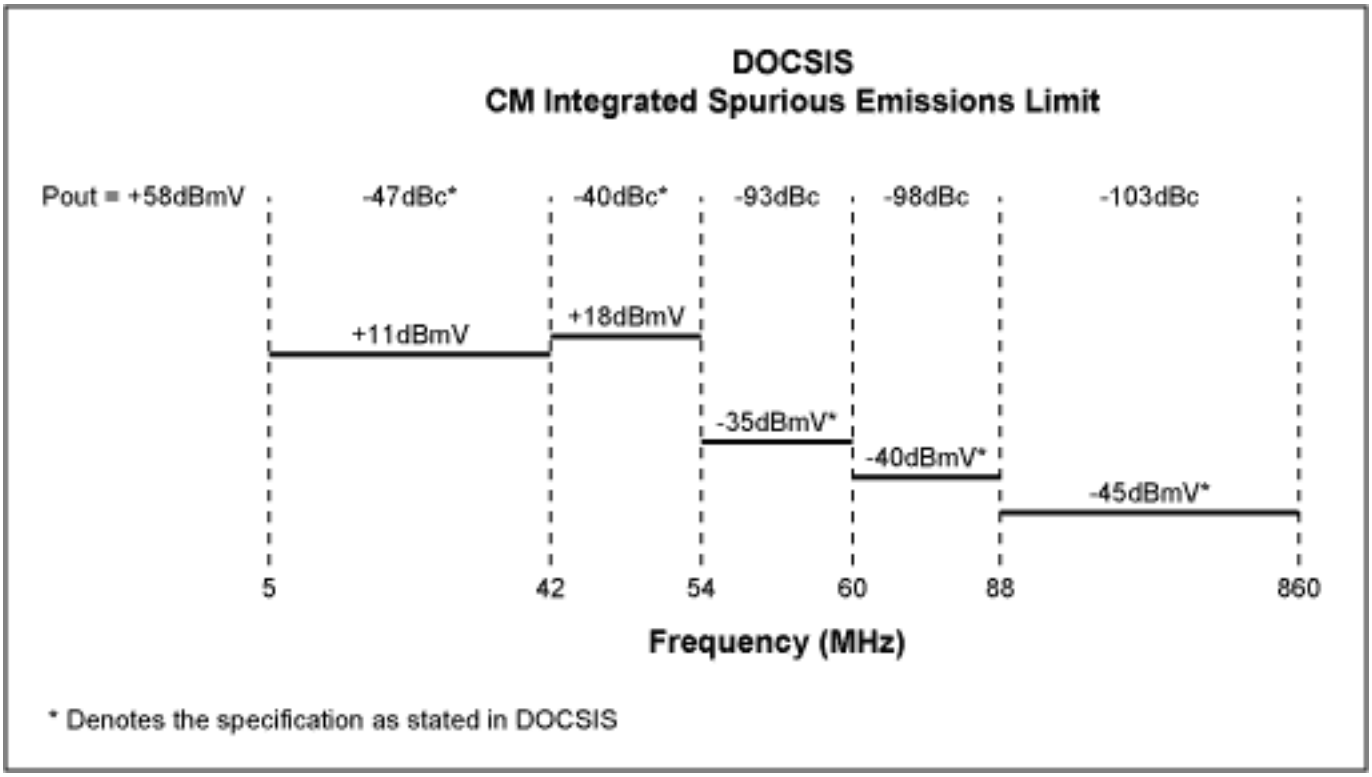

Figure 3. DOCSIS integrated spurious emissions limit

Figures 5 through 8 show harmonic distortion VS output power for 9MHz, 22MHz, 33MHz and 42MHz. 60MHz is where the DOCSIS specification drops to -40dBmV, or 98dBc (58 - -40). The MAX3509 has -53dBc at fo = 22MHz (3rd harmonic at 66MHz) at Pin = 33dBmV (See Figure 6). The duplexer will need 45dBc (98-53) at 60MHz. The other critical area for the duplexer is at 54MHz where the DOCSIS limit is -35dBmV. An 18MHz third harmonic is 54MHZ. So the

required duplexer insertion loss at 54MHz will be 40dBc (58+35-53). Make note that the third harmonic distortion is the limiting factor. The best input power would be 33dBmV or possibly lower.

Test Conditions

All tests performed at room temperature.

Output transformer Toko 458PT-1087 N=1:2.

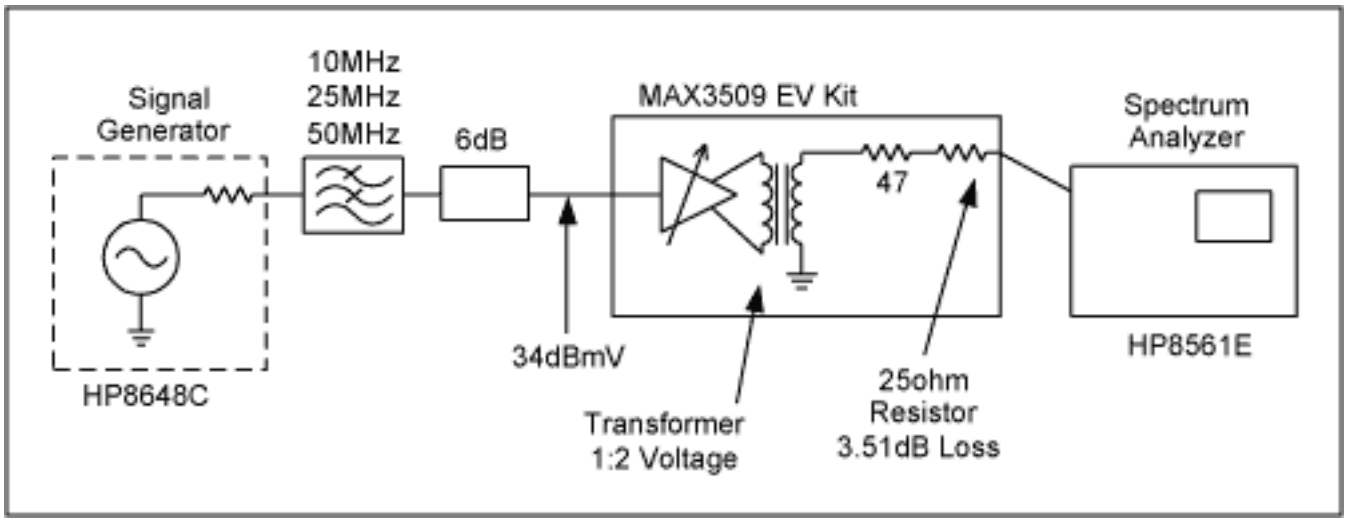

Figure 4. Test conditions diagram

Figure 5 shows 2nd and 3rd harmonic distortion data for a fundamental input frequency of 9MHz. This plot is useful to show in-band harmonics better than 59dBc at Pin = +33dBmV (third harmonic is the limiting linearity). This exceeds DOCSIS 47dBc requirements.

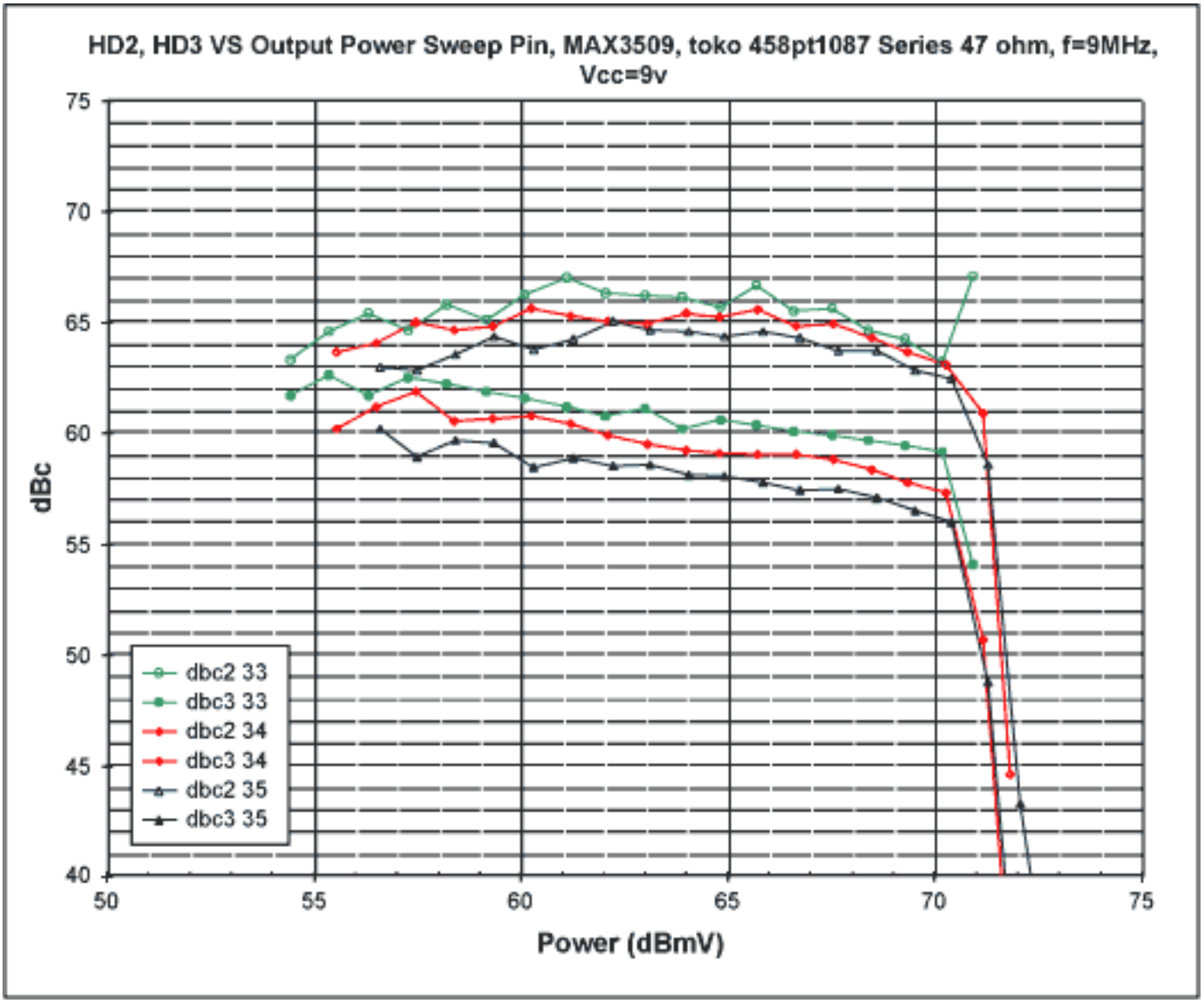

Figure 5

Figure 6 shows 2nd and 3rd harmonic distortion data for a fundamental input frequency of 22MHz. This plot is useful to show out of band harmonics better than 53dBc at Pin = +33dBmV and Pout = +67dBmV (third harmonic is the limiting linearity).

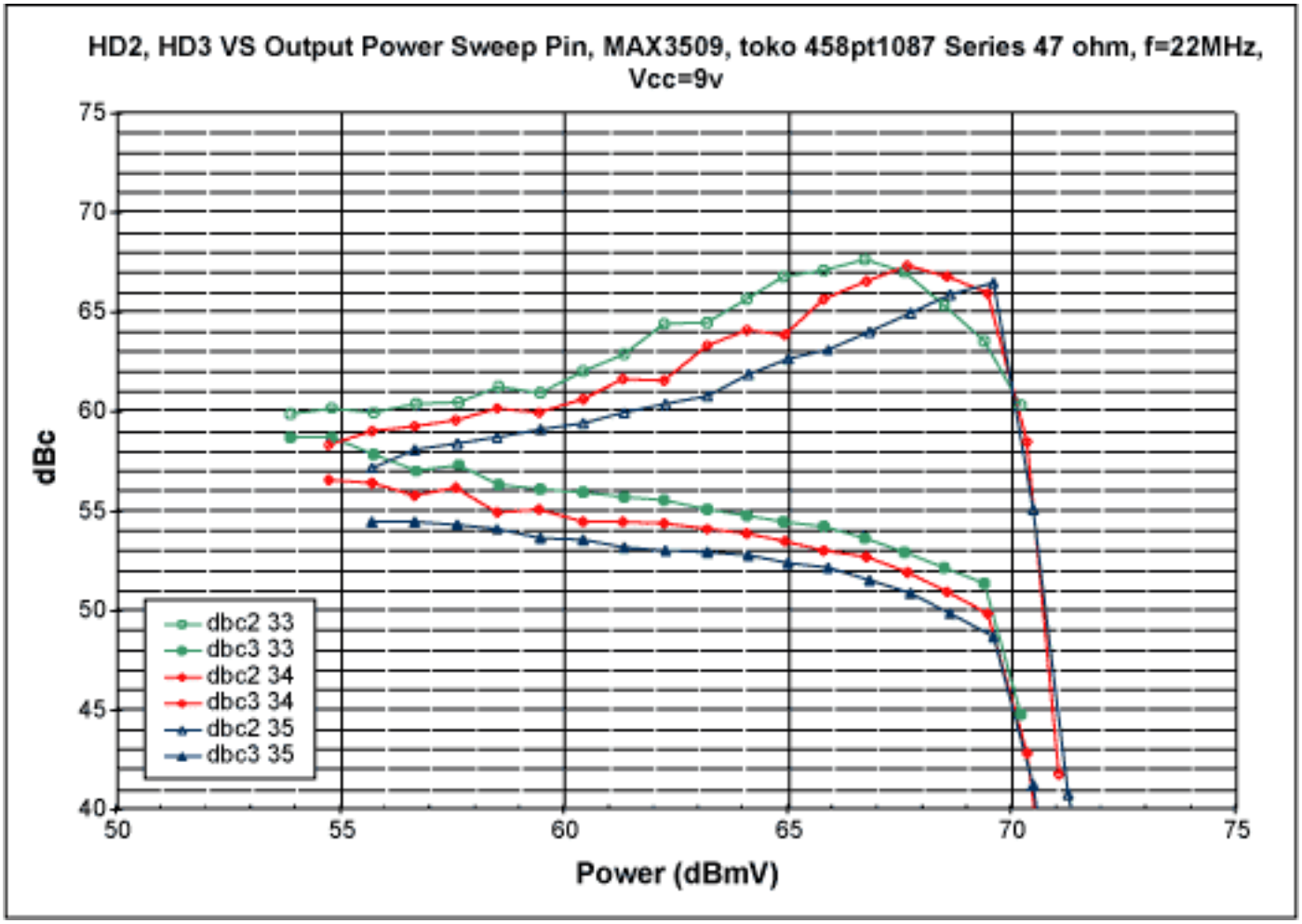

Figure 6

Figure 7 shows 2nd and 3rd harmonic distortion data for a fundamental input frequency of 33MHz. This plot is useful to show out of band harmonics better than 51dBc at Pin = +33dBmV and Pout = +67dBmV (third harmonic is the limiting linearity).

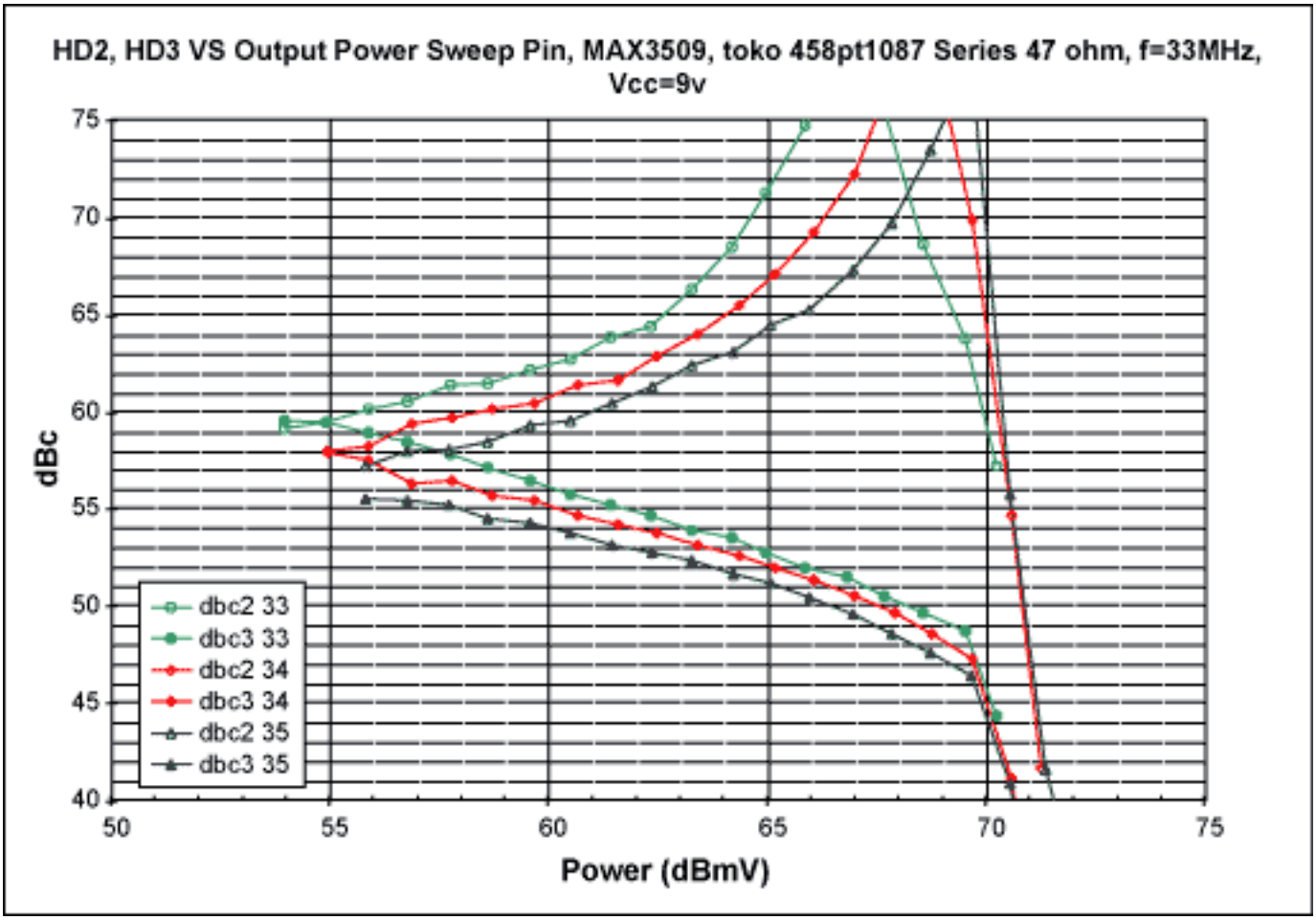

Figure 7

Figure 8 shows 2nd and 3rd harmonic distortion data for a fundamental input frequency of 42MHz. This plot is useful to show out of band harmonics better than 50dBc at Pin = +33dBmV and Pout = +67dBmV (third harmonic is the limiting linearity).

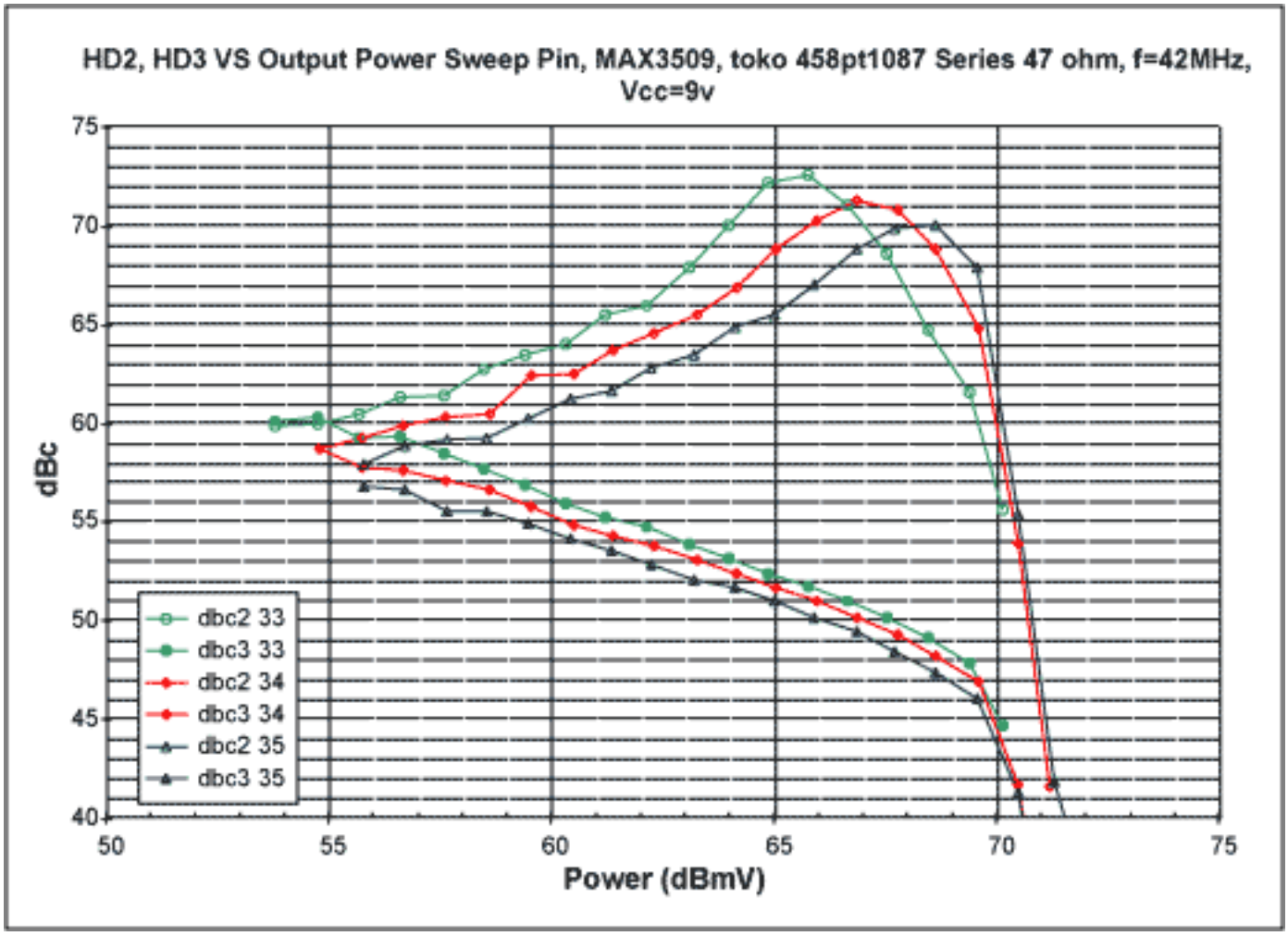

Figure 8

Figure 9 shows 3rd harmonic distortion data for several fundamental input frequencies. This plot is useful to show 3rd harmonic performance over frequency.

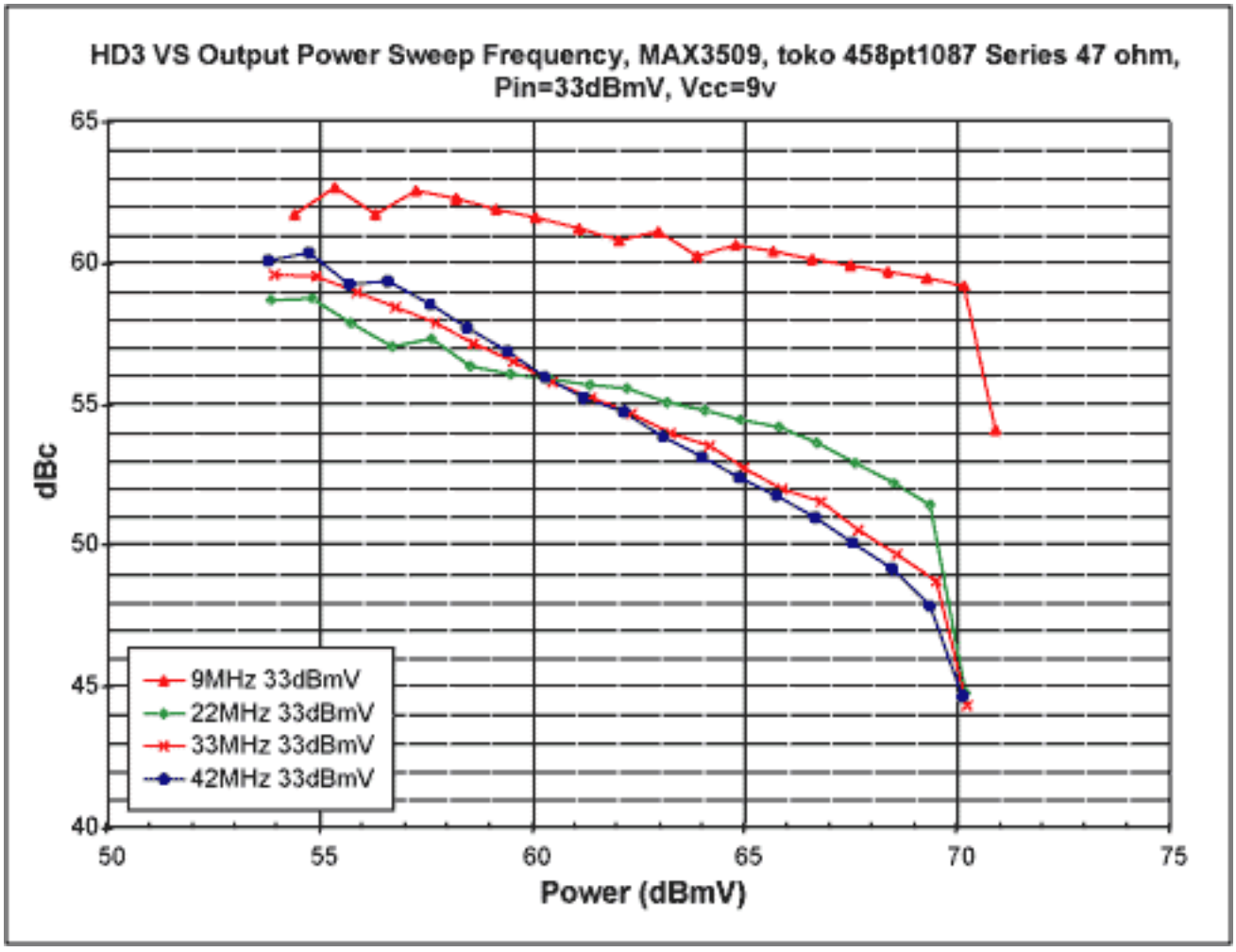

Figure 9

Figure 10 shows how 3rd harmonic distortion data changes by lowering V_{CC} to 8.3V.

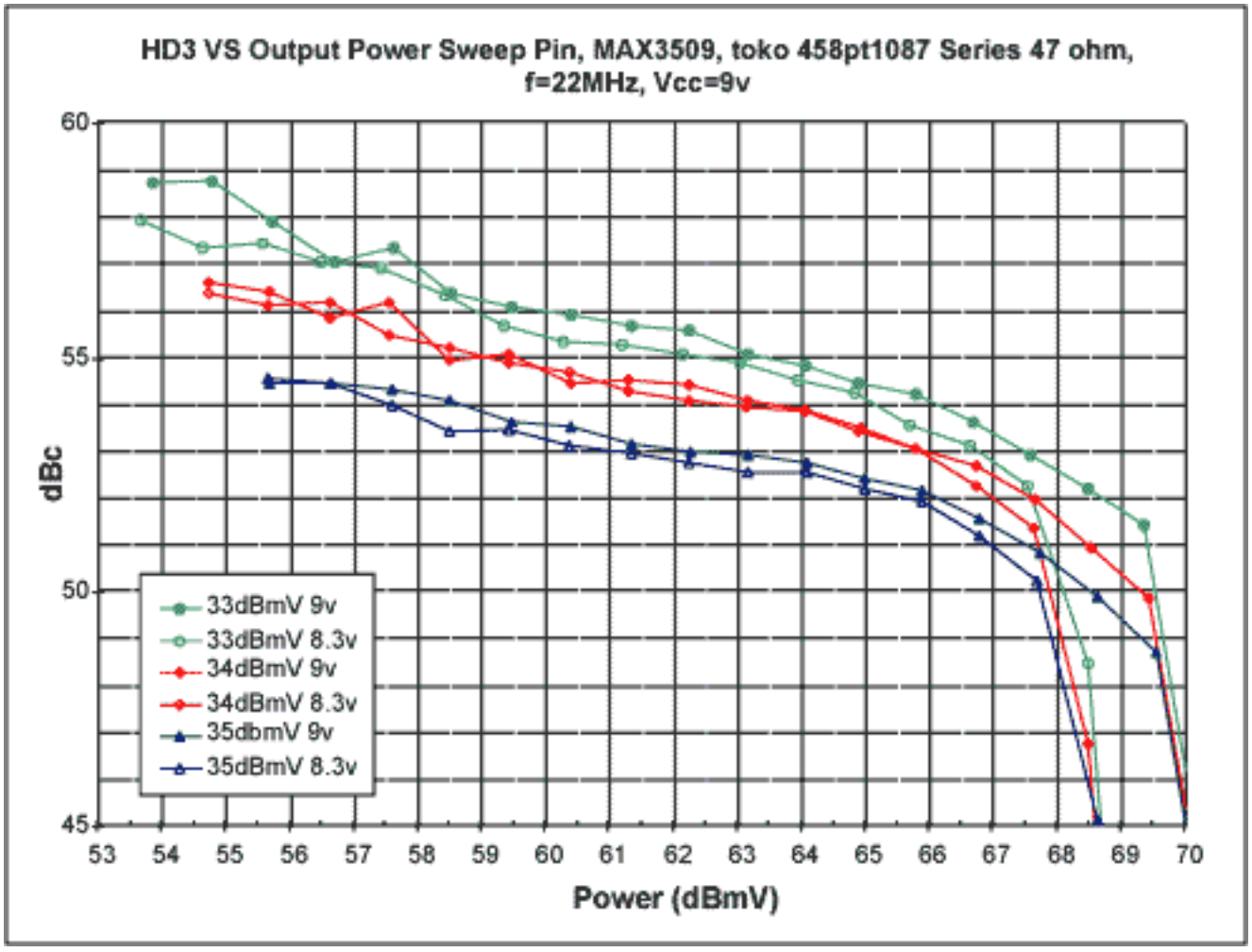

Figure 10

Figure 11 shows 100mW power savings by using V_{CC} = 8.3V.

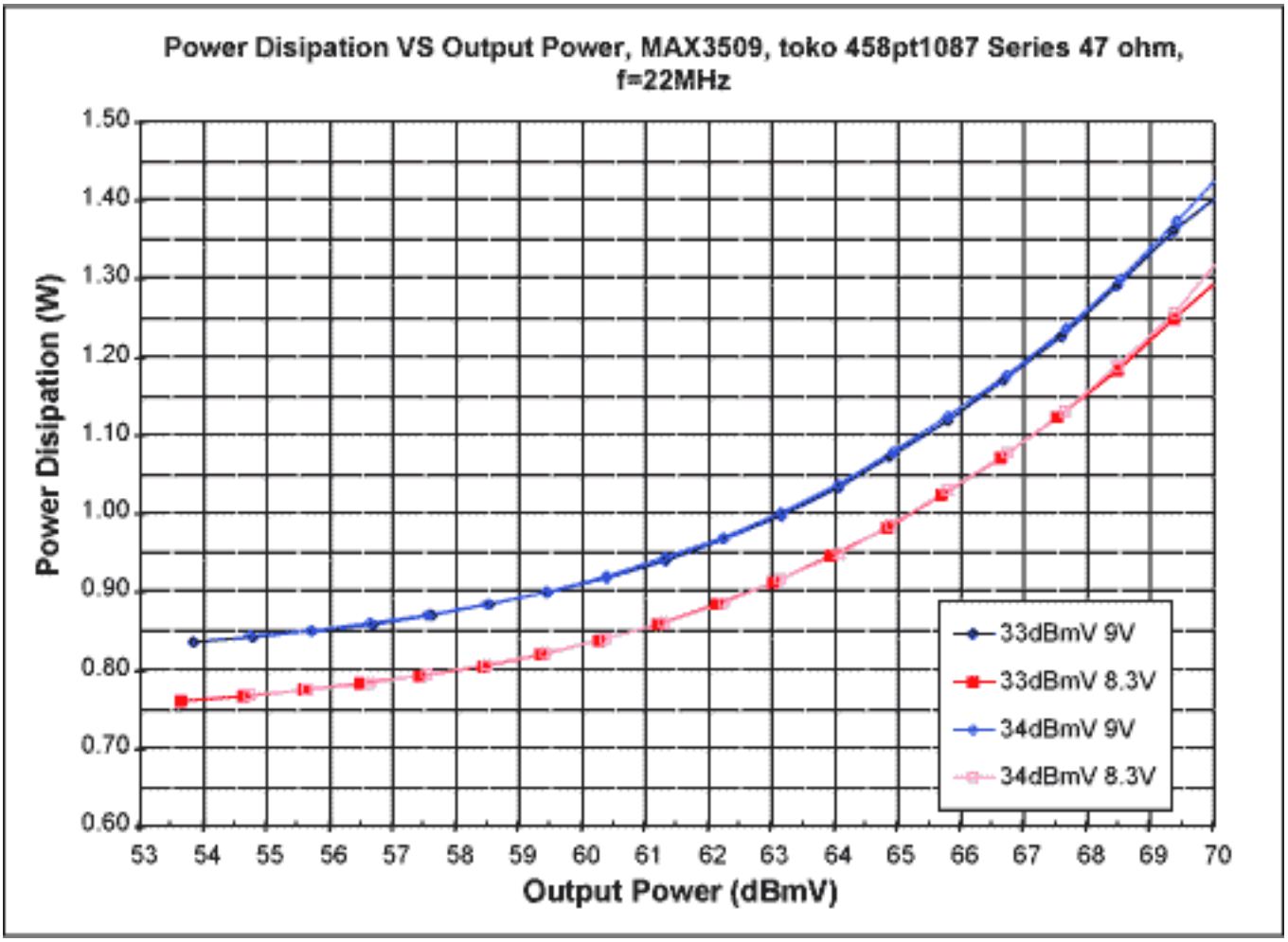

Figure 11

Figure 12 shows 100mW power savings by using V_{CC} = 8.3V.

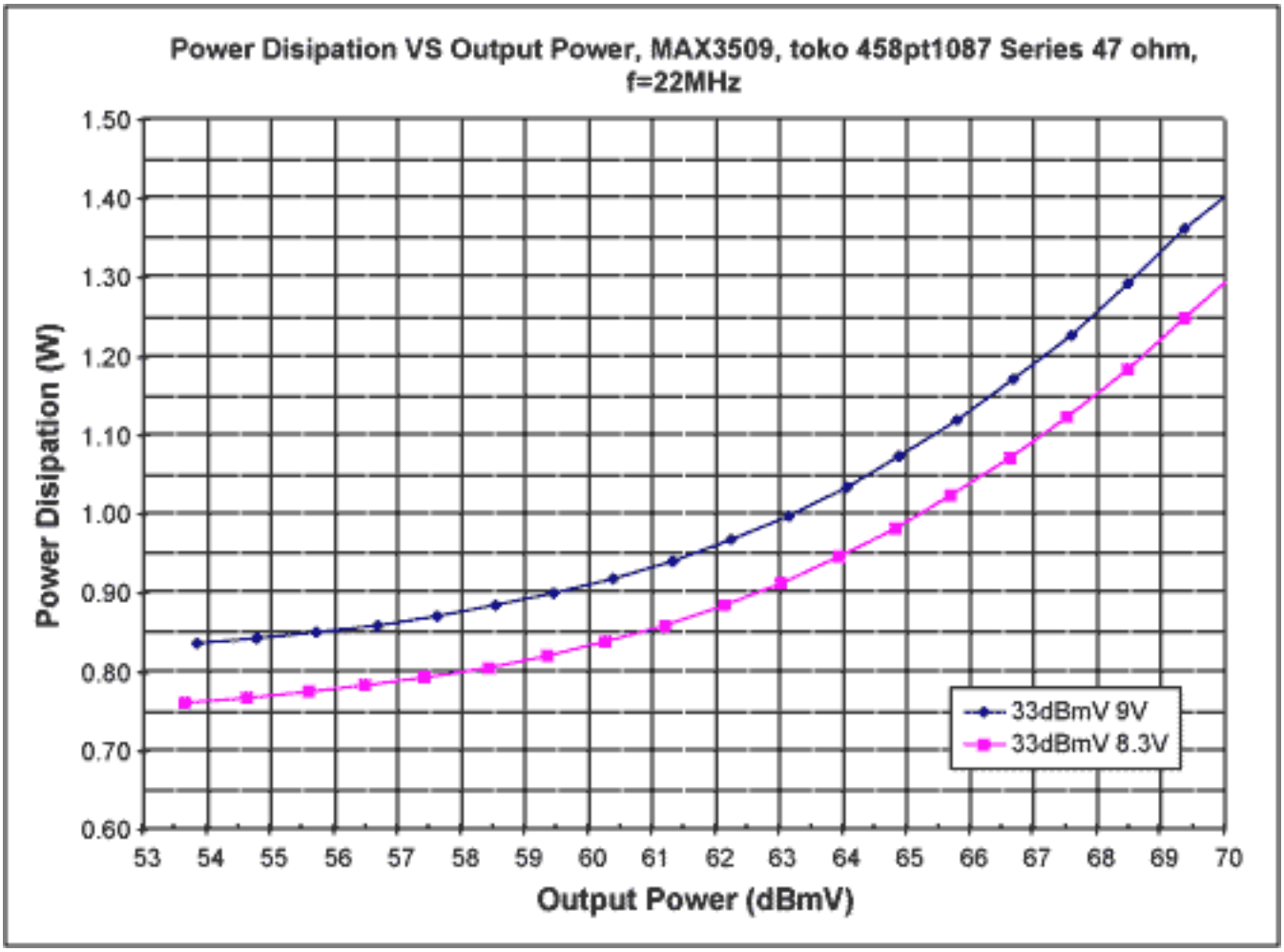

Figure 12

Figure 13 shows that small changes in V_{CC} does not effect I_{CC} very much.

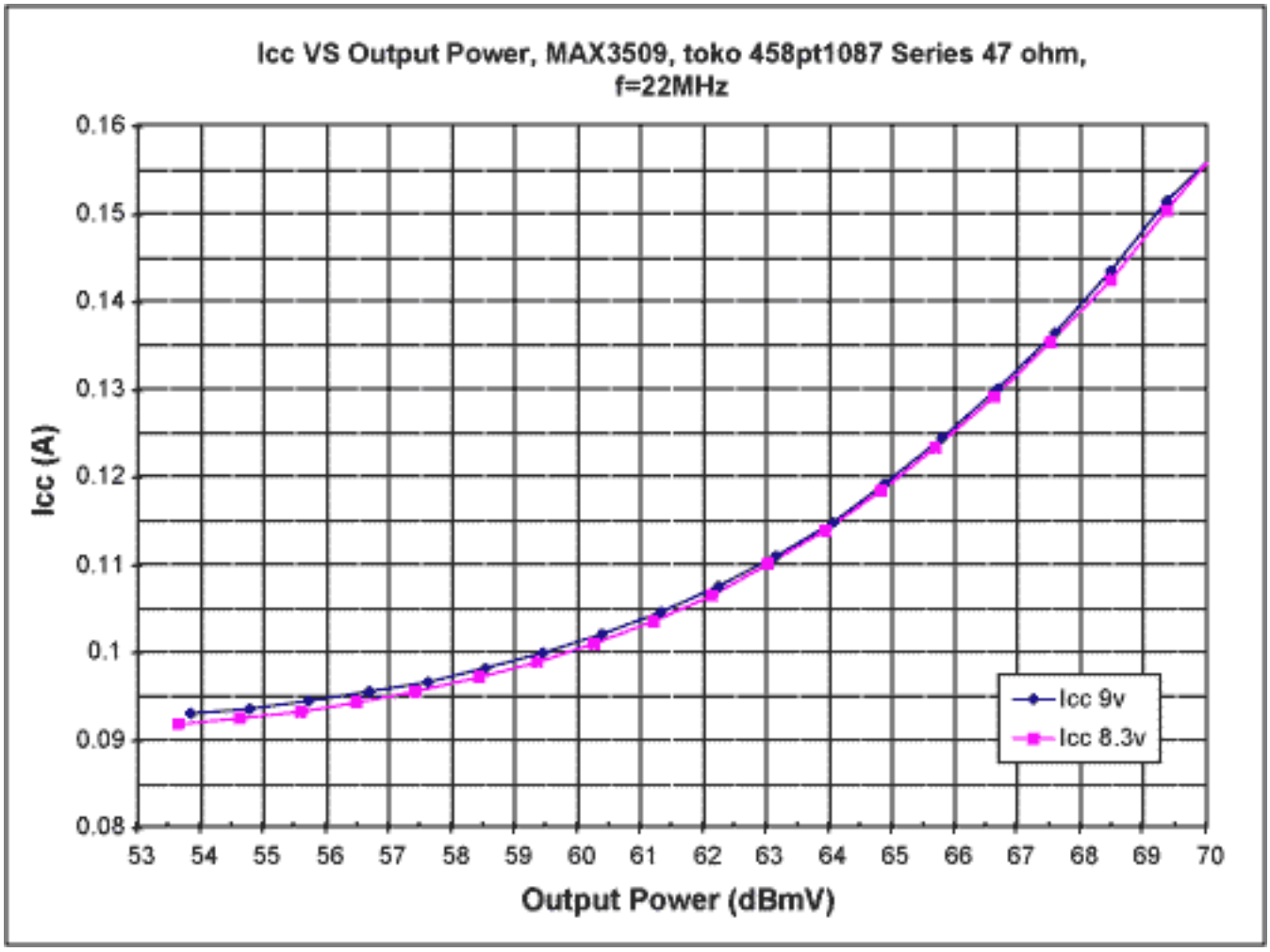

Figure 13

Conclusion

A MAX3509 can be configured (See Figure 4) to overcome coupler loss and meet DOCSIS power levels. The solution is a combination of steps:

1. Using a 1:2 output transformer to increase voltage by 6dB.
2. Adding a thermal layer to the chassis with the proper thermal resistance. This allows the MAX3509 to draw enough current for highly linear operation while in the SOA.
3. Lowering the input drive below +33dBmV to increase linearity.
4. De-rating the output power to +67dBmV for linearity.
5. Adding series output resistance to limit power dissipation of the MAX3509.

Appendix

Summary of JEDEC thermal test board specifications (JESD51-7)

The thermal test board described in this spec is most appropriate for Maxim IC applications.

Material: FR-4

Layers: 2 signals (front and backside) and 2 planes (internal)

Finished thickness: 1.60 +/- .16mm

Metal thickness- front and backside traces: 2 oz. copper (.070mm finished thickness)

- 2 internal planes: 1 oz. copper (.035mm finished thickness)

Dielectric layer thickness: 0.25mm - 0.50mm

Board size: 76.20mm x 114.30mm +/- 0.25mm for packages less than 27mm on a side.

Component Side Trace Design: Traces should be laid out so that the test device is centered on the board. Traces must extend at least 25mm from the edge of the package body. Trace widths shall be 0.25 +/- 10% for 0.5mm or greater pitch packages. For packages with finer pitches, the trace width shall equal the lead width. Trace pattern and trace termination requirements are specified in JESD51-7.

Backside Trace Design: Component side traces terminated with through hole vias may be connected to the edge connector by traces or by wire (22 AWG or smaller, copper wire). JESD51-7 specifies the current limits for different wire sizes.

Power and Ground Planes: Power and ground planes must be unbroken except for via isolation clearance patterns. The planes must not be present within 9.5mm of the edge connector pattern. Other requirements are specified in JESD51-7.

References

Maxim, MAX3509 Data Sheet Rev 0

Maxim, MAX3509 Evaluation Kit Data Sheet Rev 3

JESD51-7, High Effective Thermal Conductivity Test Board for Leaded Surface Mount

Packages, http://www.jedec.org/DOWNLOAD/search/default2.cfm

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More Information

MAX3509: QuickView -- Full (PDF) Data Sheet -- Free Samples